



U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

**SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT**

Docket Number:
10746/32

Application Number
10/092,089

Filing Date
March 5, 2002

Examiner
**Not Yet
Assigned**

Art Unit
2859

Title
CLOCK/DATA RECOVERY CIRCUIT

Applicant(s)
Keiji KISHINE et al.

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby bring the references listed on the attached modified PTO Form No. 1449 to the attention of the Examiner. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.
2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is enclosed, except as otherwise indicated.
3. It is believed that no fees are due in connection with this Information Disclosure Statement. However, should any fees be due, the Commissioner is authorized to charge Deposit Account No. 11-0600 for such fees. A duplicate copy of this communication is enclosed for charging purposes.

Dated: 8/25/2003

By: [Signature]

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**SUPPLEMENTAL
INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

ATTY. DOCKET NO.
10746/32

U.S. SERIAL NO.
10/092,089

APPLICANT
Keiji KISHINE et al.

FILING DATE
March 5, 2002

GROUP
2859

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
	6,259,755	July 10, 2001	Eugene O'Sullivan et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	5-56410	March 5, 1993	Japan			Abst.	

OTHER DOCUMENTS

EXAMINER INITIAL		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		M. Wurzer et al., "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz Silicon Bipolar Technology, "IEEE J. Solid-State Circuits, Vol. 34, No. 9, pp.1320-1324 Sep. 1999.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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